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Gate-Planarized Low-Operating Voltage Organic Field-Effect Transistors Enabled by Hot Polymer Pressing/Embedding of Conducting Metal Lines

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"Soft" electronics fabricated via new cost-effective processes will require the discovery/implementation of new materials components as well as unconventional approaches to device assembly.[1] Organic molecular and polymeric (semi)conductors and gate dielectrics are among the most important materials for this new technology since they are needed for fabricating thin-film transistors (TFTs)—the essential electronic device component.[2] Therefore, successful TFT materials candidates should be depositable via inexpensive methodologies, such as spin-coating, casting, and printing, and at low temperatures to ensure compatibility with plastic substrates. Furthermore, for complementary circuits, both p- (hole-) and n-type (electron-transporting) semiconductors should perform optimally with the same gate dielectric material. During the past few years, a number of efficient p- and n-type semiconductors for organic TFTs (OTFTs) have been discovered.[3] More recently, research in this area has attacked the problem of large OTFT operating voltages by developing new high-capacitance gate dielectric materials,[4] most of which consist of very thin films.[4b] The latter include ultrathin crosslinked polymer blend dielectrics which are solution-processable, compatible with both p- and n-type semiconductors, and enable OTFT operation at fractions of volts.[4b] However, since in these studies (and to our knowledge, in all OTFT structures based on very thin dielectrics) the gate is *unpatterned*, the crucial question arises as to whether it is possible to deposit nanoscopic dielectric films on *patterned* gate lines (essential for practical TFT circuitry) and yet preserve excellent insulating characteristics, high dielectric strength, and smooth surface morphology. This issue is even of greater importance for printed conductors since the features are invariably thicker than for conventional vapor-deposited metal patterns.[1f]

In this contribution, we demonstrate a new methodology for fabricating patterned, gate-planarized, polymer insulator-based TFTs operating at low voltages — hot polymer pressing/embedding. Processes of this general type[5] have the advantage of low fabrication temperatures and scalable manufacturing applicability. We show here that pressing polymeric foils or powders at temperatures above the glass transition temperature (T_g) onto prepatterned conducting features allows transfer, after cooling, of the patterned conductor from the substrate "donor" to the polymeric film. The result is a new flexible plastic substrate fabricated in situ in which the film surface exposes self-planarized gate lines. Polymer dielectric and semiconductor films can then be deposited with great uniformity, avoiding partial/irregular gate coating and catastrophic pinholes typically arising from shadow effects caused by protruding gate lines.

Proof-of-concept experiments were carried out on a locally fabricated hot-press consisting of a bottom Al block heater and an upper weighted steel press head (Figure 1A). TFT device fabrication begins with hot-pressing/embedding of the conducting gate lines (Figure 1B). A Si (or smooth glass) donor substrate with vapor-deposited Al or Au or printed Ag particle ink (Acheson Colloids) features is placed on the Al heater block, and PMMA powder (or

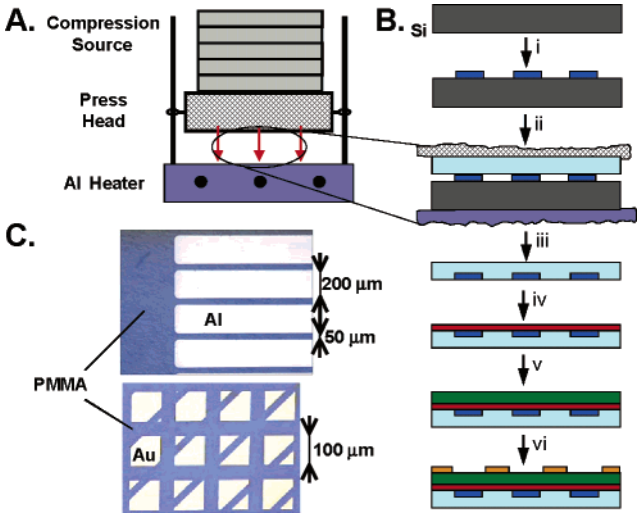

Figure 1. (A) Schematic of the polymer pressing/embedding setup. (B) TFT fabrication process scheme: (i) conducting gate line deposition/patterning (blue) on the substrate donor (gray); (ii) hot-pressing of polymer foil/powder (light blue); (iii) peel-off of polymer-embedded gate lines, yielding OFET gate-substrate; (iv) spin-coating deposition of the **PVP**−$\mathbf{C_6}$ dielectric (red layer); (v) deposition of semiconducting layer (green); (vi) deposition of source-drain electrodes (orange). (C) Reflection optical micrograph of Al gate lines and Au features embedded in poly(methyl methacrylate) (PMMA).

film) is dispersed (positioned) on top. The steel block is brought into contact, and upon heating to the desired process temperature (140−180 °C, > the PMMA T_g), a small pressure (∼300−400 KPa) is applied by placing weights on the steel block. Pressure is maintained for the time required to ensure uniform conductor embedding, which depends on whether the polymer film/powder is preheated. After cooling below T_g, the new composite PMMA−conductor substrate is detached from the Si wafer/glass donor. To facilitate detachment, the substrate donor surface is treated with $CF_3(CF_2)_9(CH_2)_2SiCl_3$ vapor before line deposition to yield a low surface energy self-assembled monolayer. Note that the same substrate can be used multiple times. Figures 1C and S1−S3 show examples of the diverse metal features that can be embedded in PMMA via this process. The metal transfer/embedding yield is quantitative with Al and Au and currently >90% with printed Ag patterns. Feature sizes as small as 15 μm to >1.0 cm are readily transferred (limited by our shadow mask/printing capabilities), and there are no reasons to believe that even narrower features cannot be processed. For OTFTs, a 20−200 nm thick **CPVP**−$\mathbf{C_6}$ dielectric layer (crosslinked polymer blend)[4a] is next deposited by spin-coating a mixture of poly(vinylphenol) (PVP) and α,ω-bis(trichlorosilylhexane) crosslinking reagent in EtOH. The TFT device structure is completed by depositing the semiconductor layer (50 nm) and finally vapor-depositing Au source-drain electrodes (50 nm).

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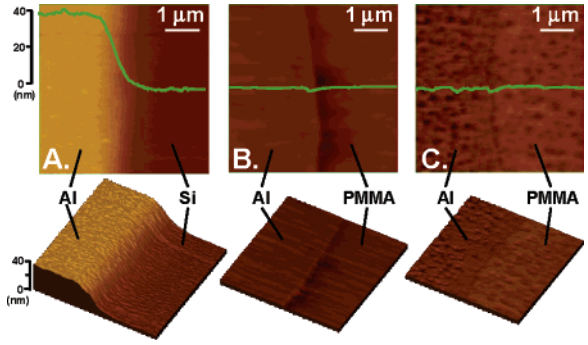

Figure 2. AFM images of (A) Al line sidewall vapor-deposited on Si; (B) Al−PMMA interface after hot-pressing/embedding and detaching from the substrate. (C) The same interface after spin-coating a thin **CPVP−C$_6$** layer. The green line indicates the height profile.

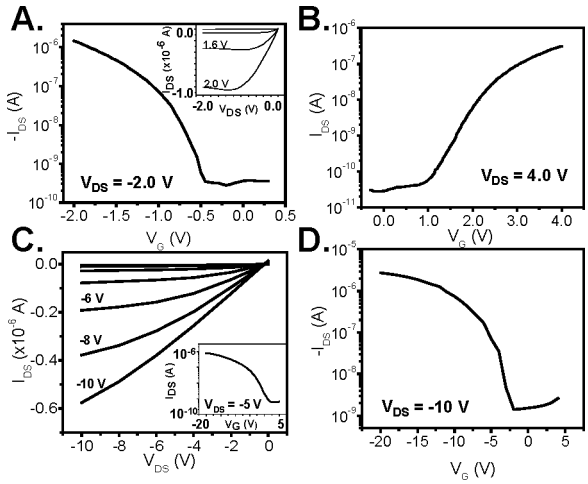

Figure 3. Current−voltage plots and response of the following devices: (A) Al/**PVP−C$_6$** (C_i = 260 nF/cm^2)/pentacene/Au (L/W = 100/5000 μm); (μ_{sat} = 0.18 cm^2 V^{-1} s^{-1}); (B) Al/**PVP−C6** (C_i = 260 nF/cm^2)/**DFHCO-4T**/Au (L/W = 100/5000 μm); (μ_{sat} = 0.02 cm^2 V^{-1} s^{-1}); (C) Au/**PVP−C$_6$** (C_i = 25 nF/cm^2)/pentacene/Au (L = 100 μm, W = 500 μm); (μ_{sat} = 0.04 cm^2 V^{-1} s^{-1}); (D) Ag/**PVP−C$_6$** (C_i = 9 nF/cm^2)/pentacene/Au (L/W = 100/1000 μm); (μ_{sat} = 0.27 cm^2 V^{-1} s^{-1}).

Atomic force microscopic (AFM) images of the conductor−polymer substrate interface demonstrate the effectiveness of this process in transferring conductor lines and in achieving gate planarization. Figure 2A shows an AFM image of a 40 nm thick Al line sidewall on a Si substrate. After hot-pressing and peel-off, the Al−PMMA interface is planarized with an rms roughness < 0.9 nm (Figure 2B). On this planarized surface with embedded Al features, a 17 nm thick dielectric film can be deposited with great uniformity over the same interface (rms roughness < 1.5 nm, Figure 2C). Note that for all metals, the conductor−polymer interface is planarized and extremely smooth (Figure S4). Currently, the minimum dielectric thickness that has been deposited on these materials is ∼20 (Al), ∼100 (Au), and ∼200 nm (Ag), and therefore the maximum dielectric capacitance [C_i (nF/cm^2)] is ∼280 (Al), ∼40 (Au), and ∼12 (Ag),[6] respectively; it depends on the bulk roughness, intrinsic wettability, and chemical characteristics of the embedded feature. Leakage current−voltage measurements of (Al, Au, Ag)/insulator/Au (vapor-deposited) metal−insulator−metal (MIM) structures demonstrate excellent **CPVP−C$_6$** insulating properties on patterned gate-planarized lines, with all leakage current densities <10^{-5} A/cm^2 at 1 MV/cm (Figure S5).

OTFTs fabricated as described above demonstrate the broad applicability of this process to yield low-voltage patterned gate devices. Figure 3 shows representative output and transfer plots using various gate materials and semiconductors. Al gate-based OTFTs with a ∼20 nm thick **PVP−C$_6$** dielectric operate at a few volts. The results obtained using this type of device with pentacene (p-type, Figure 3A) and α,ω-di(1-perfluorohexylcarbonyl) quaterthiophene (**DFHCO-4T**,[3c] n-type, Figure 3B) demonstrate compatibility with both types of semiconducting materials. Pentacene OTFTs with Au (Figure 3C) and Ag (Figure 3D) gates also function at low voltages, demonstrating materials gate generality.

In conclusion, a new methodology for fabricating patterned, gate-planarized OTFTs based on hot polymer pressing/embedding has been demonstrated. This technique is applicable to a variety of gate conductors and polymer matrices,[7] and the resulting devices function at low voltages with a variety of semiconductors, suggesting new routes to flexible printed electronics.

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Supporting Information Available: Device/film fabrication details. Figures S1−S6. This material is available free of charge via the Internet at http://pubs.acs.org.

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(6) The C_i of Ag-based MIM structures is lower than that calculated from the **CPVP−C$_6$** thickness and *k*. This is probably the result of thermoplastic resins used in the Ag ink composition which increase the effective thickness between the Au top electrodes and Ag bottom particles.

(7) This approach has also been successful for hot-pressing/embedding using poly(vinylpyrrolidone) and polystyrene as well as embedding using various poly(dimethylsiloxane) polymers (Figure S6).

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